

## CLAIMS

We claim:

- 1           1.     A method of simulating a circuit comprising:  
2               representing a plurality of identical components in a reduced form as  
3     a circuit having a single instance of the identical component with encoding  
4     for each input of the single instance to represent corresponding inputs to all  
5     of the plurality of identical components and decoding for each output port  
6     of the single instance to create output ports for the corresponding outputs  
7     associated with all of the plurality of identical components; and  
8               symbolically simulating the reduced form of the circuit with  
9     simulation results being the same as results of symbolically simulating the  
10    plurality of identical components.
  
- 1           2.     The method defined in Claim 1 wherein the circuit comprises n  
2     signals having  $2^n$  states, and further wherein encoding the circuit produces  
3     simulation run time data structures asymptotically smaller than n.

1           4.       The method defined in Claim 1 wherein each input port of the  
2   reduced form of the circuit is mapped to an encoded port and each output  
3   value is decoded back to a set of values of corresponding outputs of the  
4   plurality of identical components, where each value in the set of values  
5   corresponds to an output of one of the plurality of identical components.

1           6.       The method defined in Claim 4 wherein each output i of the  
2   single instance of the identical component in the reduced form represents  
3   the output i for each component in the plurality of identical components.

1           7.     The method defined in Claim 1 wherein each component in the  
2     plurality of identical components comprises a plurality of identical  
3     subcircuits, and the single instance of the identical component in the  
4     reduced form includes a single instance of the identical subcircuit.

1           8.     The method defined in Claim 1 wherein input encoding in the  
2     reduced form is generated by applying binary encoding to inputs of the  
3     plurality of identical components.

1           9.     The method defined in Claim 1 wherein input encoding in the  
2     reduced form is generated by applying ternary encoding to inputs of the  
3     plurality of identical components.

1           10.    The method defined in Claim 1 wherein symbolically  
2     simulating the reduced form of the circuit is performed using Binary  
3     Decision Diagram (BDD).

1           11.    The method defined in Claim 1 wherein the components  
2   comprise one or more selected from the group consisting of a net, a port, an  
3   array, and a memory.

1           12.    The method defined in Claim 1 wherein at least one of the  
2   components comprises at least one signal having a plurality of states.

1           13.    An apparatus of simulating a circuit comprising:  
2           means for representing a plurality of identical components in a  
3   reduced form as a circuit having a single instance of the identical component  
4   with encoding for each input of the single instance to represent  
5   corresponding inputs to all of the plurality of identical components and  
6   decoding for each output port of the single instance to create output ports  
7   for the outputs associated with all of the plurality of identical components;  
8   and  
9           means for symbolically simulating the reduced form of the circuit  
10   with simulation results being the same as results of symbolically simulating  
11   the plurality of identical components.

1           14.    The apparatus defined in Claim 13 wherein the circuit  
2   comprises  $n$  signals having  $2^n$  states, and further wherein encoding the  
3   circuit produces simulation run time data structures asymptotically smaller  
4   than  $n$ .

1           15.    The apparatus defined in Claim 13 wherein the circuit  
2   comprises  $n$  signals having  $2^n$  states, and further wherein encoding the  
3   circuit produces simulation run time data structures asymptotically close to  
4    $\log(n)$ .

1           16.    The apparatus defined in Claim 13 wherein each input port of  
2   the reduced form of the circuit is mapped to an encoded port and each  
3   output value is decoded back to a set of values of outputs of the plurality of  
4   identical components, where each value in the set of values corresponds to  
5   an output of one of the plurality of identical components.

1           17.    The apparatus defined in Claim 16 wherein each input  $i$  of the  
2   single instance of the identical subcircuit in the reduced form of each input  $i$   
3   represents the input  $i$  for all of the plurality of identical subcircuits.

1           18.    The apparatus defined in Claim 16 wherein each output i of the  
2   single instance of the identical component in the reduced form represents  
3   the output i for each component in the plurality of identical components.

1           19.    The apparatus defined in Claim 13 wherein each component in  
2   the plurality of identical components comprises a plurality of identical  
3   subcircuits, and the single instance of the identical component in the  
4   reduced form includes a single instance of the identical subcircuit.

1           20.    The apparatus defined in Claim 13 wherein input encoding in  
2   the reduced form is generated by applying binary encoding to inputs of the  
3   plurality of identical components.

1           21.    The apparatus defined in Claim 13 wherein input encoding in  
2   the reduced form is generated by applying ternary encoding to inputs of the  
3   plurality of identical components.

1           22.    The apparatus defined in Claim 13 wherein symbolically  
2    simulating the reduced form of the circuit is performed using Binary  
3    Decision Diagram (BDD).

1           23.    The apparatus defined in Claim 13 wherein the components  
2    comprise one or more selected from the group consisting of a net, a port, an  
3    array, and a memory.

1           24.    The apparatus defined in Claim 13 wherein at least one of the  
2    components comprises at least one signal having a plurality of states.

1           25.    An article of manufacture having one or more recordable  
2    media to store executable instructions which, when executed by a processing  
3    device, cause the processing device to:  
4            represent a plurality of identical components in a reduced form as a  
5    circuit having a single instance of the identical component with encoding for  
6    each input of the single instance to represent corresponding inputs to all of  
7    the plurality of identical components and decoding for each output port of

